

PRODUCT SPECIFICATION

Part No.:	AC-XF-8G10-01	
Description:	10G XFP Transceiver, MMF 850nm 300m	
Release Date	Rev.	Revision Change Description
2016/07/16	A0	New Release
2020/12/28	A1	Template Update

Features

- ✧ XFI Loopback Mode
- ✧ Supports 9.95Gb/s to 11.3Gb/s bit rates
- ✧ Power dissipation <1.5W
- ✧ Uncooled 850nm VCSEL laser
- ✧ Duplex LC receptacle optical interface compliant
- ✧ Single +3.3V power supply
- ✧ Hot-pluggable XFP footprint
- ✧ Maximum link length 300m over OM3 MM Fiber
- ✧ No Reference Clock required
- ✧ Operating temperature range:
 - ✧ Commercial: 0°C~+70°C
 - ✧ Industrial: -40 ~ +85°C
- ✧ RoHS Compliant
- ✧ Built-in digital diagnostic functions
- ✧ Standard bail release mechanism

Application

- ✧ 10GBASE-SR/SW 10G Ethernet
- ✧ 1200-Mx-SN-I 10G Fiber Channel

Standard

- ✧ Compliant with XFP MSA
- ✧ Compliant with SFF-8472
- ✧ Compatible with IEEE802.3ae

Specification

Absolute Maximum Ratings				
Parameter	Symbol	Min	Max	Unit
Storage temperature	TS	-40	85	°C
Power Supply Voltage	Vcc	-0.5	+4	V
Relative Humidity	RH	5	95	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Operating Case Temperature	Standard	0		+70	°C
	Industrial	-40		+85	°C
Power Supply Voltage	Vcc	3.13	3.30	3.47	V
Power Supply Current	Icc			640	mA
Data Rate			10.3	11.3	Gbps
Fiber Length 50µm core MMF		-	300	-	m

Electrical Characteristics						
Parameter	Symbol	Min	Typical	Max	Unit	Notes
Transmitter differential input voltage		120		1000	mV	
Receiver differential output Voltage		600	650	800	mV	
Input differential impedance	R		100		Ω	
Transmit Disable Assert Time			10		us	
Transmit Fault (TX_Fault)	Voh	2		Vcc	V	LVTTTL
	Vol	0		0.8	V	LVTTTL
Loss of Signal (LOS)	Voh	Vcc-0.5		Vcc	V	LVTTTL
	Vol	0		0.5	V	LVTTTL
TX Disable	Vih	2		Vcc	V	LVTTTL
	Vil	0		0.8	V	LVTTTL

Optical transmitter Characteristics						
Parameter	Symbol	Min	Typical	Max	Unit	Notes
Launched Power (avg.)	Pout	-6		-1	dBm	
Operating Wavelength Range	λc	840	850	860	nm	
Spectral Width (RMS)	Δλ			0.45	nm	
Extinction Ratio	ER	3	5		dB	2
Relative Intensity Noise	RIN			-128	dB/Hz	
Optical Rise/Fall Time	Tris/Tfall		40		PS	3

Transmitter and Dispersion Penalty	TDP			3.9	dBm	
Output Eye Diagram	Complies with IEEE802.3z eye masks when filtered					
Optical receiver Characteristics						
Parameter	Symbol	Min	Typical	Max	Unit	Notes
Receiver Sensitivity	S			-10	dBm	4
Wavelength Range	λ_c	840		860	nm	
Optical Power Input Overload	P_{in-max}	+0.5			dBm	4
Receiver Reflectance	R			-12	dB	
LOS	Optical De-assert	P_d		-12	dBm	4
	Optical Assert	P_a	-30			
LOS hysteresis		0.5		5	dB	5

Notes:

- 1) The supply current is XFP module's working current.
- 2) For the measurements, the device was driven with 10Gbps data pattern with $2^{31}-1$ PRBS payload.
- 3) Optical transition time is the time interval required for the rising or falling edge of an optical pulse to transition between the 20% and 80% amplitudes relative to the logical 1 and 0 levels
- 4) Measured with a PRBS $2^{31}-1$ test pattern, @10Gbps, ER=3dB, BER< 10^{-12}
- 5) The LOS Hysteresis minimizes 'chatter' on the output line. In principle, Hysteresis alone does not guarantee chatter-free operation.

Digital Diagnostic Memory Map

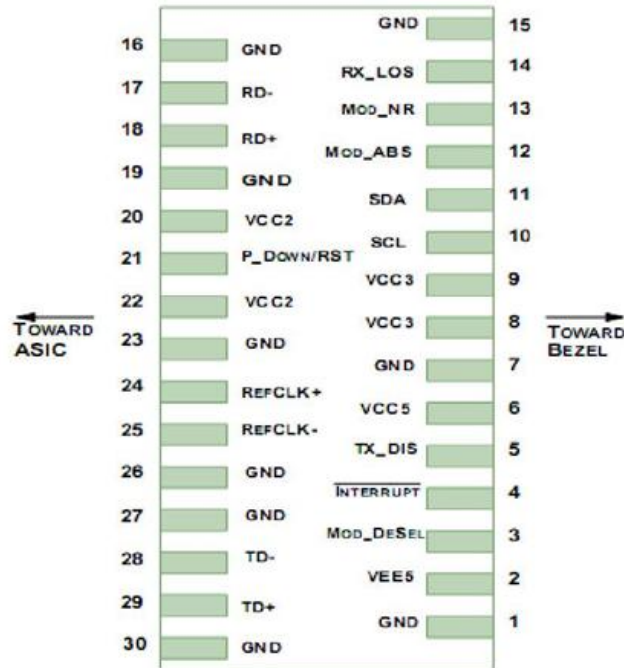
As defined by the XFP MSA, LONTE XFP transceivers provide digital diagnostic functions via a 2-wire serial interface, which allows real-time access to the following operating parameters:

- Transceiver temperature
- Laser bias current
- Transmitted optical power
- Received optical power
- Transceiver supply voltage

It also provides a sophisticated system of alarm and warning flags, which may be used to alert end-users when particular operating parameters are outside of a factory-set normal range.

The operating and diagnostics information is monitored and reported by a Digital Diagnostics Transceiver Controller (DDTC) inside the transceiver, which is accessed through the 2-wire serial interface. When the serial protocol is activated, the serial clock signal (SCL pin) is generated by the host. The positive edge clocks data into the XFP transceiver into those segments of its memory map that are not write-protected. The negative edge clocks data from the XFP transceiver. The serial data signal (SDA pin) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially. The 2-wire serial interface provides sequential or random access to the 8 bit parameters, addressed from 000h to the maximum address of the memory.

Pin Descriptions



Pin Assignment

Pin	Signal Name	Description	Plug Seq.	Notes
1	GND	Module Ground		1
2	VEE5	Optional -5.2 Power Supply – Not required		
3	Mod-Desel	Module De-select; When held low allows the module to respond to 2-wire serial interface commands	LVTTTL-I	
4	Interrupt	Interrupt (bar); Indicates presence of an important condition which can be read over the serial 2-wire interface	LVTTTL-O	2
5	TX_DIS	Transmitter Disable; Transmitter laser source turned off	LVTTTL-I	
6	VCC5	+5 Power Supply		
7	GND	Module Ground		1
8	VCC3	+3.3V Power Supply		
9	VCC3	+3.3V Power Supply		
10	SCL	Serial 2-wire interface clock	LVTTTL-I	2
11	SDA	Serial 2-wire interface data line	LVTTTL-I/O	2
12	Mod_Abs	Module Absent; Indicates module is not present. Grounded in the module.	LVTTTL-I	2
13	Mod_NR	Module Not Ready; XGIGA defines it as a logical OR between RX_LOS and Loss of Lock in TX/RX.	LVTTTL-I	2
14	RX_LOS	Receiver Loss of Signal indicator	LVTTTL-I	2
15	GND	Module Ground		1

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16	GND	Module Ground		1
17	RD-	Receiver inverted data output	CML-O	
18	RD+	Receiver non-inverted data output	CML-O	
19	GND	Module Ground		1
20	VCC2	+1.8V Power Supply – Not required		
21	P_Down/RST	Power Down; When high, places the module in the low power stand-by mode and on the falling edge of P_Down initiates a module reset. Reset; The falling edge initiates a complete reset of the module	LVTTTL-I	
22	VCC2	including the 2-wire serial interface, equivalent to a power cycle. +1.8V Power Supply – Not required		
23	GND	Module Ground		1
24	RefCLK+	Reference Clock non-inverted input, AC coupled on the host board – Not required	PECL-I	3
25	RefCLK-	Reference Clock inverted input, AC coupled on the host board – Not required	PECL-I	3
26	GND	Module Ground		1
27	GND	Module Ground		1
28	TD-	Transmitter inverted data input	CML-I	
29	TD+	Transmitter non-inverted data input	CML-I	
30	GND	Module Ground		1

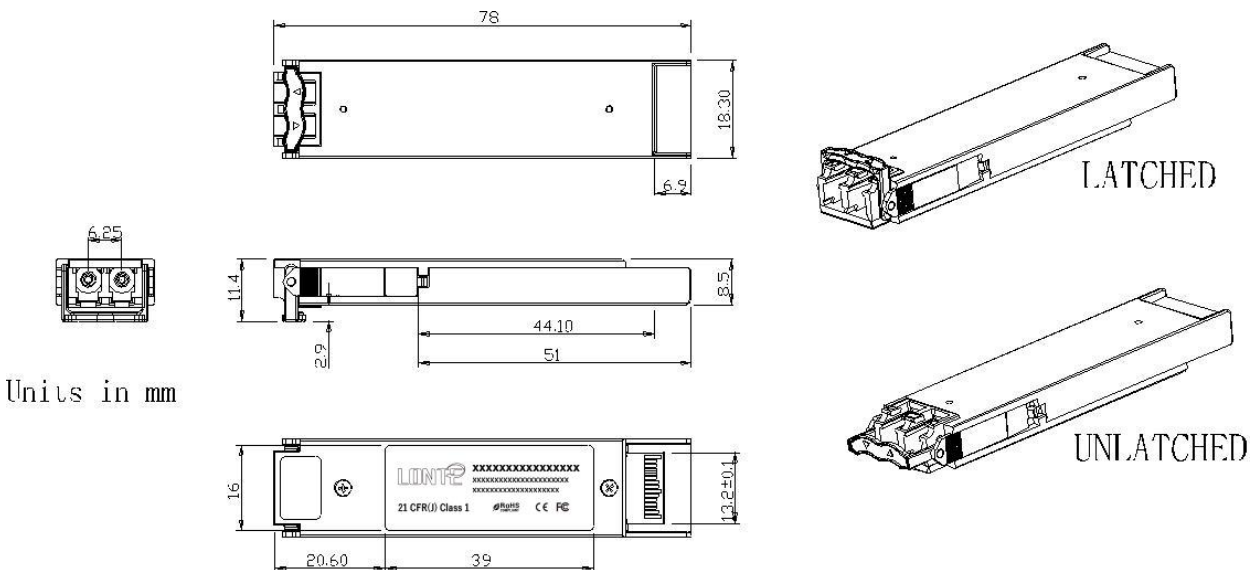
Notes:

Plug Seq.: Pin engagement sequence during hot plugging.

- 1) Module circuit ground is isolated from module chassis ground within the module.
- 2) Open collector; should be pulled up with 4.7k – 10kohms on host board to a voltage between 3.15V and 3.6V.
- 3) A Reference Clock input is not required by the AC-XF-8G10-01. If present, it will be ignored.

Package Outline

Dimensions are in millimeters. All dimensions are ±0.2mm unless otherwise specified. (Unit: mm)



Units in mm

Regulatory Compliance

Feature	Test	Method
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883E Method 3015.7	Class 1 (>1.5kV) – Human Body Model
Electrostatic Discharge (ESD) Immunity	IEC61000-4-2	Class 2(>4.0kV)
Electromagnetic Interference (EMI)	CISPR22 ITE Class B FCC Class B CENELEC EN55022 VCCI Class 1	Comply with standard
Immunity	IEC61000-4-3	Comply with standard
Eye Safety	FDA 21CFR 1040.10 and 1040.11 EN (IEC) 60825-1,2	Compatible with Class I laser Product

Ordering information

Part. No	Specifications								
	Pack	Rate (Gbps)	Tx (nm)	Po (dBm)	RX	Sen (dBm)	Temp (°C)	Reach (m)	DDM
AC-XF-8G10-01	XFP	10.3125	850	-6~-1	PIN	<-10	0~70	300	Y
AC-XF-8G10-01F	XFP	10.3125	850	-6~-1	PIN	<-10	-40~85	300	Y